HAOYANG LI

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EDUCATION

Southern University of Science and Technology **Shenzhen, China**
Bachelor of Engineering
Microelectronics Science and Engineering August 2022 – June 2026
• Overall GPA: 3.94/4.0 Ranking: **1/127** (Among all students majoring in Microelectronics at SUSTech)

University of California, Berkeley **Berkeley, U.S.A**
Visiting Student
Department of Electrical Engineering and Computer Sciences August 2024 – May 2025
• GPA: 4.0/4.0
• Undergraduate researcher at Prof. Robert Pilawa's research group

University of California, San Diego **La Jolla, U.S.A**
Visiting Student
Department of Electrical and Computer Engineering May 2025 – September 2025
• Undergraduate researcher at Prof. Prasad Gudem's research group
• Research on capacitor cubing circuits and exploring their applications in both digitally controlled oscillators (DCOs) for digital phase-locked loops (PLLs) and ultra-high-Q RF filters.

HONORS

• Outstanding Student Scholarship, Second Prize (top 10%) 2023, 2024
• The second "Material Art" Competition, Second Prize 2022

RESEARCH INTERESTS

Analog and Mixed-Signal Integrated Circuits Design

PUBLICATIONS

[1] A New Y-function MOSFET Mobility Extraction Method Accounting for Coulomb Scattering at Cryogenic Temperatures
Shilong Li, Chengbo Yang, Hao Su, **Haoyang Li**

- **Accepted by 8th Sino MOS-AK Workshop 2024. (August 2024)**
- **Under Review: International Journal of Numerical Modelling: Electronic Networks, Devices and Fields**

RESEARCH EXPERIENCE

48V-12V Hybrid Dickson Converter for Split-Phase Control UC Berkeley
Advisors: **Prof. Robert Pilawa** (Department of Electrical Engineering and Computer Sciences) Nov. 2024 – Mar. 2025

- Conducted comprehensive simulations in LTSpice to analyze soft-charging dynamics, split-phase control, topology trade-offs, and design optimizations for hybrid switched-capacitor converters.
- Designed PCBs using Altium Designer, focusing on component optimization, commutation loop minimization, and modular testability for testing flexible-timing split-phase control.
- Contributed to the development and validation of innovative Fibonacci-Dickson fusion topologies for high-efficiency power conversion.

A New Y-function MOSFET Mobility Extraction Method at Cryogenic Temperatures SUSTech
Advisors: **Prof. Kai Chen** (School of Microelectronics, SUSTech) Oct. 2023 - Jun. 2024

- Derived the equations to extract different parameters including low-field mobility, effective mobility, the first, second, third degeneration coefficients. Using MATLAB to process MOSFET I-V data, perform computational analysis, apply linear fitting, and adjust fitting parameters to ultimately obtain the desired parameters.
- Paper link: https://www.mos-ak.org/xian_2024/ (**Accepted, fourth Author**)

Testing of the bandgap reference circuit SUSTech
Advisors: **Prof. Junmin Jiang** (Department of Electrical and Electronic Engineering, SUSTech)
June. 2024 - July. 2024

- Studied the working principles of the bandgap reference circuit.
- Tested the functionality of the operational amplifier and ADC blocks.
- Used a Raspberry Pi to generate PWM signals for chip heating during testing.

ACADEMIC PROJECTS

Fully Integrated WiFi6 Baseband PGA + Low-Pass Filter Design UC Berkeley

Advisors: **Prof. Osama Shana'a** (IEEE Fellow, Senior Director at MediaTek)

- Developed a fully integrated PGA and lowpass filter targeting 10 MHz and 20 MHz WiFi6 baseband channels.
- Full of 15 specifications, including 3dB-bandwidth, voltage gain (0dB-14dB), gain step (2dB), filter rejection, noise, linearity (P1dB, IM3), DC offset, settling time, shutdown leakage current, common-mode input/output voltage, and minimize power consumption.
- Incorporated common-mode feedback for robust DC operating point and differential signal integrity.
- Packaged using a 28-pin QFN. Assigned all pin functions and designed the SPI interface.
- All specs are met under nominal operating points, and most of them are met over PVT.

Synchronous Buck Converter for Maximum Power Point Tracking (MPPT) UC Berkeley

Advisors: **Prof. Jessica Boles** (Department of Electrical Engineering and Computer Sciences)

- Designed and laid out a synchronous buck converter in Altium Designer for photovoltaic maximum power point tracking (MPPT) applications.
- Built and validated a loss model including switching, conduction, winding, and core losses.
- Sized components for ripple specs and hand-wound a custom inductor.
- Assembled, debugged, and tested hardware across operating conditions.
- Implemented a closed-loop MPPT algorithm (Perturb and Observe) using a TI C2000 microcontroller.

Operational Amplifier Design for Smartwatch LCD Driver UC Berkeley

Advisors: **Prof. Rikky Muller** (Department of Electrical Engineering and Computer Sciences)

- Designed a two-stage amplifier with high gain and high output swing.
- Implemented in Cadence Virtuoso with a 45nm CMOS process.
- Sized transistors using the gm/I_D methodology.

Tetris Game on FPGA Using the Verilog HDL Programming Language SUSTech

Advisors: **Prof. Fengwei An** (School of Microelectronics)

- Implemented the Tetris game on an FPGA using Verilog, including features such as game start and pause, block falling, left/right movement, rotation, line clearing, and score display.
- Modularized the testbench (including IP Core and PLL verification) and validate basic functionality through simulation.
- Successfully validated key functionalities on the FPGA, ensuring system reliability.

SELECTED COURSES

Analog Integrated Circuits (A)
*Advanced Analog Integrated Circuits (In Progress)
Power Electronics (A)
Power Electronics Design (In Progress)
Introduction to MEMS and NEMS (A)
Semiconductor Material Physics (A)
Signals and Systems (A+)
Semiconductor for Devices and Packaging (A)
Advanced Microelectronics Experiment I(A)
Advanced Microelectronics Experiment II(A+)
Electromagnetic Field and Electromagnetic Waves(A+)
Semiconductor Device (A+)
*Si-based Quantum Computing Cryogenic CMOS(A)

** Represent graduate-level courses*

EXTRACURRICULAR ACTIVITIES & INTERESTS

- Member of the Dormitory Management Committee at SUSTech Sep. 2023 – Aug. 2024
- Volunteer at the 6th Working Meeting of the Teaching Advisory Committee for Marine Science Programs in Higher Education Sep. 2023
- Champion of the 6th Fun Sports Meet at the Zhixin College Sep. 2023
- Outstanding Individual in the "Winter Break Alumni Homecoming" at SUSTech Jan. 2024

SKILLS

Programming: MATLAB, C, Python, Assembly Language (RISC-V)

Design and Simulation Tools: Cadence Virtuoso, Altium Designer, KiCad, LTspice, PLECS, Silvaco TCAD